REMARKS

In the Office Action, the Examiner rejects claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over Okumura (U.S. 4935380) in further view of the admitted prior art (APA) of the subject patent application and (U.S. 5605854). The applicant has carefully reviewed both the Okumura '380 as well as the U'854 references and is familiar with the APA. The applicant respectfully notes the following differences between the combined teachings of the Okumura '380 and U '854 references as well as the APA.

Particularly, Okumura discloses a variety of methods of forming semiconductor devices having a lightly doped drain/source structure (LDD). As discussed in the personal interview between the Examiner and the applicant's undersigned representative on February 3, 2005, several embodiments of the Okumura devices disclose an intermediate step in the formation of the Okumura devices wherein a pad oxide layer is positioned on an underlying silicon substrate and further overlaid by a polysilicon layer, then a silicide layer with an uppermost polysilicon layer (see for examples Figure 7a, 8a, 9a, and 10a. However, the Applicant respectfully notes that the process/methods of Okumura proceed quite differently than the Applicant's claimed invention as described below. The Applicant believes that the embodiments of Okumura illustrated and described with respect to figures 10a-10h and 11a-11f are most analogous to the method of the applicant's claimed invention including forming a local interconnect.

With respect to the embodiments illustrated and described with respect to figures 10a-10h, the Applicant respectfully directs the Examiner's attention to the particular description of this method of Okumura at columns 12 and 13. As illustrated in figure 10e the uppermost layer of the gate stacks comprises the silicon system material pattern 408 which is previously described as comprising polysilicon. A heat treatment is carried out in the semiconductor substrate 401 for form impurity regions 416 having low impurity concentration and impurity regions 417 having high impurity concentration having the conductivity type opposite to the semiconductor substrate and these regions constitute together with the polysilicon gate, a LDD device. In this heat treatment, the silicon system material pattern 408 reacts with the atoms of oxygen reaching the surface thereof to turn itself to a silicon oxide film 418. The oxidation reaction prevents the formation of a porous oxide film layer on the silicide pattern 407 of a metal having a high melting point, so that the degradation of the electrical characteristics of the

polycide gate transistor, especially the increase of heat resistance of the gate, increase of contact resistance on the gate from the upper layer interconnection can be prevented (Figure 10f) (*See,* Column 12, Lines 49-59). Thus the applicant respectfully notes that Okumura '380 specifically teaches and suggests that the upper layer of the gate stack comprises the silicon oxide film 418 to improve the circuit performance of the Okumura '380 devices. The applicant further notes that when the polysilicon 421 is subsequently positioned as illustrated in figure 10h of Okumura the insulating film 419 partially covers the upper surface of the gate stack and the partially exhumed region of the upper surface of the gate stack contacted by the polysilicon 421 comprises the silicon oxide film 418. While the silicon oxide film obviously comprises silicon it can in no way be considered to be silicon rich source layer contacted by an overlaid refractory material as in the applicant's claimed invention.

The applicant further notes the teachings of the embodiment Okumura '380 illustrated and described with respect to figures 11a-11f. The applicant notes that Okumura discloses at column 13 line 1 "meanwhile, one object of the present invention to provide a structure which prevents formation of a porous oxide film layer on the silicide of a metal having high melting point in heat treatment for diffusing implanted impurities. Therefore it goes without saying that the material is not limited to the silicon system material. An embodiment employing a silicon oxide as the material is disclosed in the following as a still-further embodiment." In this embodiment, an oxide film is formed on the semi-conductor substrate 401 and a polysilicon 403 is deposited thereon. A silicide 404 of a metal having a high melting point is deposited thereon and a silicon oxide film 423 is deposited further thereon. (*c.f.* Column 13, Lines 17-23). This structure is then patterned and etched to form the silicon oxide film pattern 424 as illustrated in Figures 11B-11H such that, again, the upper surface of the gate stack of this embodiment of Okumura '380 comprises silicon oxide. This silicon oxide is contacted by the polysilicon 421 and again in no way discloses or suggests placing a refractory material in contact with a silicon-rich source layer for formation of silicided contacts at exhumed portions of a gate stack.

Similarly, the Yoo '854 reference teaches structures and methods for forming an LDD MOSFET. In the Yoo reference '854 a gate oxide layer 16 is formed on the semiconductor substrate 10 and is further overlaid by a polysilicon layer and a tungsten silicide layer. (*See,* Figure 1). This structure is then patterned and etched to form a gate stack with spacers 24. The

LDD n regions are ion implanted and driven by an annealing process in oxidizing ambient such as O_2 or H_2O at a temperature of between about 900 to 950° C. for between 25 to 35 minutes. (Column 3, Lines 12-24). Along with driving in the LDD impurities, this annealing process forms a silicon dioxide layer over the horizontal surfaces of the substrate as shown in Figure 5. The silicon dioxide layer is formed to a thickness 28 of between about 60 to 120 Angstroms over the semiconductor substrate and to a thickness 30 of between about 500 to 600 Angstroms over the tungsten silicide layer 20. A layer of titanium 32 is then deposited over the substrate including over the gate stack and then a rapid thermal annealing (RTA) is performed in a nitrogen ambient such as N_2 or NH_3 at a temperature of between about 650 to 750° C. Thus, in Yoo' 854 as well, the upper surface of the gate stack comprises silicon dioxide of the thickness 30 which is then overlaid with the titanium layer 32. Again, while the silicon dioxide atop the gate stack of Yoo '854 comprises silicon, it can in no way be considered a silicon-rich source for further reaction with the titanium. Yoo '854 specifically notes that the titanium overlying the gate structure reacts with the nitrogen ambient to form titanium nitride overlying the gate structure whereas formation of a titanium silicide is restricted to the region 34 located well beyond the gate structure.

The Applicant respectfully reminds the Examiner that the APA illustrates and describes an exhumed surface 202 of the gate stack 204A wherein the exhumed surface 202 corresponds to the upper surface of the laterally conducted tungsten silicide layer 210. A refractory metal, such as titanium is deposited above the substrate 208 such that the refractory metal layer 218 contacts both the exhumed surface 202 of the gate stack 204 and the active region 206 of the substrate 208. The Applicant notes, however, that as described in the APA the tungsten silicide surface 202 is a relatively poor source of silicon and, thus, the transformation of the refractory metal to a refractory metal silicide results in underproduction of titanium silicide during the annealing process resulting in a contact at the exhumed surface which is excessively reactive during the following wet etch leading to the indicated undercuts.

Thus, as described above, the Applicant strongly believes that the teachings of Okumura '380, Yoo '854, and the APA taken independently or in any possible combination fail to teach or suggest the aspects of the Applicant's invention as claimed in the subject application as currently amended of "forming a gate stack on a substrate, the gate stack having at least one conductive

layer and a source layer positioned on top of the at least one conductive layer and at an uppermost surface of the gate stack, the source layer providing a rich source of transforming atoms; exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit node; depositing a refractory material so that the refractory material contacts the exposed upper-most portion of the source layer of the gate stack and so that the refractory material is also positioned to contact a second circuit node of the integrated circuit having a rich source of the transforming atoms; forming a masking layer over the refractory material; etching the masking layer so as to define an extent of the local interconnect; and selectively transforming the refractory material underneath the etched masking layer and at least adjacent the exposed portion of the source layer and the second circuit node into low resistance contacts comprising the refractory material..." (Claim 1 as currently amended). The Applicant notes that similar amendments are made to the other independent Claim 20 by this paper. Thus, the Applicant believes that Claims 1 and 20 are patentable under the requirements of 35 U.S.C. § 103(a) over the combined teachings of Okumura, Yoo, and the APA. The Applicant believes that the remaining claims depending from the independent claims 1 or 20 respectively properly further define the claimed invention and are also patentable under the requirements of 35 U.S.C. § 103(a) over the cited art.

SUMMARY

From the foregoing, the Applicant believes that the subject application as amended by this paper is patentable under the requirements of 35 U.S.C. § 103(a) over the combined teachings of Okumura, Yoo and the APA. The Applicant thus believes the application is in a condition ready for allowance and respectfully requests prompt issuance of a Notice of Allowability. However, should there remain any further impediments to the allowance of this application that might be resolved by a telephone conference, the Examiner is respectfully requested to contact the Applicant's undersigned representative at the indicated telephone number.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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